Preternatural Low-Power Reversible Decoder Design in 90 nm Technology Node

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Abstract— In Low Power VLSI Technology IC designers have encountered more constraints High speed, Small silicon area, and High throughput and Low Power dissipation. Designer is faced problem for this issue and technology doesn't advance at the same rate. Reinvent a design for Building a great interest. Reversible logic gives a solution for this issue because it has ideally zero power consumption and prevents the loss of information which is the root cause of power dissipation. In this way and optimized low power decoder and two New high speed Reversible Gates 'RG_1' and 'RG_2'are proposed by connecting this improvement of power dissipation. An epitome design methods is Reversible Gates, in reversible the number of inputs is equal to the number of outputs, allow for prevision of all succeeding states based on known retiring state, and the system ambit every potential state, termination is no heat dissipation. In this paper synthesis the reversible decoder using Xilinx platform and operative coded design is to be simulated on simulation software (e.g.Isim). Employed properly for dynamic input befitting output obtained and also reversible decoder is compelled on MOS synthesis using Tanner14 EDA tools

Index Terms— Reversible Decoder, Constant Input, Garbage Output, Total Logical Calculation, Low Power VLSIC, 3-T XOR, etc.

1 INTRODUCTION

A new epitome for VLSI is Reversible because researchers pike the world are working awkward to federalization the heat dissipation of VLSI Chips for low power consumption without conciliatory on Speed, Power and Area etc. If less amount of heat dissipates in chip due to do not loss any bit and lost bit is exactly equal to kTln2 heats dissipate where k is Boltzmann constant and T is temperature [2]. Now a inquiring in recent premise increase component density with decrease in area, heat dissipation and power consumption has a growing field in VLSI. Reversible has screeched this problem [1]. Reversible has same number of input and output it is one to one correspondence between input and output so at a time output bit engender the input. It is called inverse property of reversible gate and it is also spying error detection in output bit [6] so we said that it has no fan out problem and it has zero power dissipation if a reversible circuit is used.

The whole paper is organized as two part First part propose a Novel Reversible Gate 'RG_1' and 'RG_2'.And then design a reversible 2to4 decoder and 3to8 decoder using Xilinx platform and Simulated output is verified by simulation tools Isim.

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And second section design a Reversible 2to4 decoder in Transistor level and simulated analog circuit in Tanner 14 EDA tools simulator of tanner is T-Spice and Output waveform is visualized on W-Edit waveform viewer.

2 Literature Survey of Reversible Logic Gates

After Reversible logic windy and spying its fumigation in low power VLSI design, Quantum computing, DSP and signal processing etc. and give silver bullet to Speed, Power and Area etc. There are various reversible logic gates are procurable that are succor for designing of assorted gate in terms of Low power, Total computational cost [7,8] and the output bit generate the input bit without any lost of information and no heat is generated. Reversible handiness Gate are Feynman Gate (CNOT Gate), Fredkin Gate, and SC Gate etc.

2.1 Fredkin Gate

This Gate has three input A.B and C and also has three output P,Q and R and the Boolean expression and pictorial Gate representation shown below P = A, Q = A′B+AC, R = A′C+AB

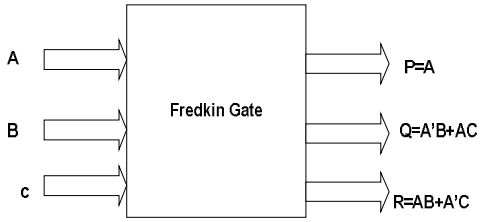


Fig. 1. Fredkin Gate

Total Logical Calculation= 2*XOR Gate+4*AND Gate+1*NOT

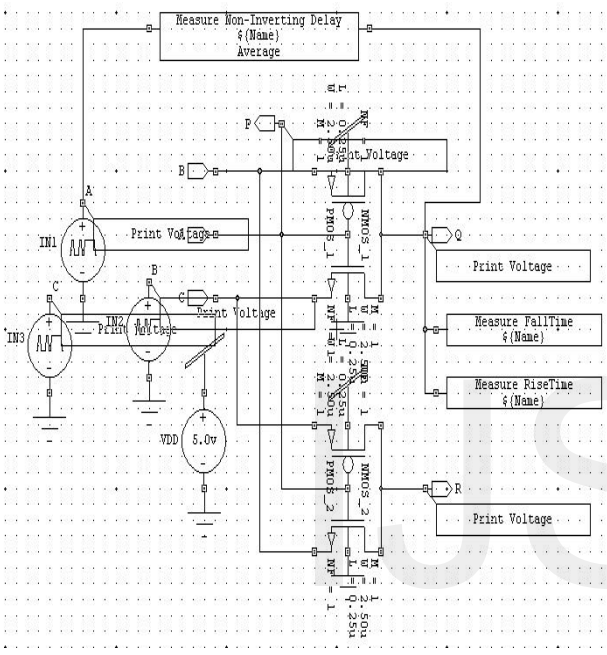


Fig 2. MOS Implementation of Fredkin Gate

2.2Feynman Gate

This Gate has two input and also two output for condition of reversibility let output is P and Q are the Boolean expression and pictorial gate representation shown below P = A, Q = A ⊕ B

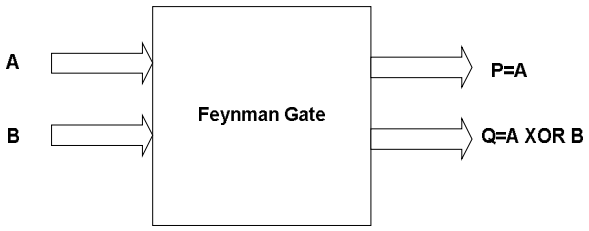


Fig 3. Feynman Gate

Total Logical Calculation= 1*XOR Gate+1*BUFFER

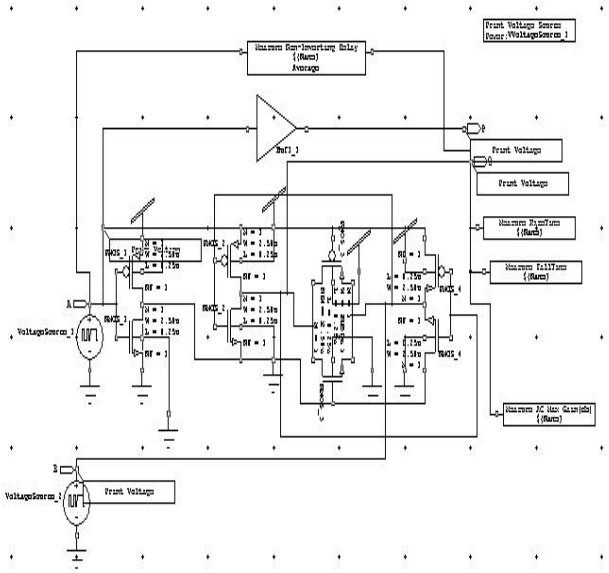


Figure 4. MOS Implementation of Feynman Gate

2.3 SC Gate

This Gate has Four input and also Four output for condition of reversibility let output is P, Q, R and S and the Boolean expression and pictorial gate representation Shown below

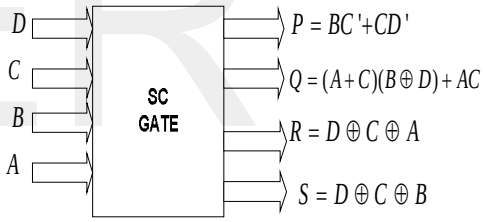


Fig 5. SC Gate

3 Related Work of Reversible Logic

Related work is categories as First propose a Two new Reversible Gate called 'RG_1' and 'RG_2' RG_1 Gate not performing the logic operation NAND, Full adder and full substractor. For performing operation of Full adder and Full substractor we propose a RG_2 Gate and then design a Reversible decoder using fredkin Gate and synthesis this design on two different platform Xilinx ISE 14.7 and Tanner 14 EDA tools and also describes Conception of Reversible Decoder and deduct the transposition of Quantum Cost and Total logical calculation for Reversible Decoder and check the simulation sequel in Xilinx platform using Virtex 7 low power Device family with speed grade -1 in section second .Section third delineate the Transistor implementation of Reversible decoder and Incision shown that simulation dissection based on Tanner 14 EDA tools and last section conclusion.

4 PROPOSED WELL BALANCE 4*4 REVERSIBLE GATES

If In this paper, propose Two new 4*4 reversible gates, called "RG_1" and "RG_2". The gates are shown with their block diagrams, consisting of inputs and outputs, along with their respective Truth Tables. The truth table of RG_1 gate is given in Table 1. Showing that every input vector has unique output vector, and that no input or output combinations are repeated.
Inputs= (A, B, C, D)
Outputs= (P, Q, R, S)

Table 1 Truth table of Propose RG_1 Gate

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	1	0	1
0	0	0	1	0	1	0	0
0	0	1	0	0	0	1	0
0	0	1	1	0	1	1	1
0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	1	0	0
1	0	1	1	1	0	1	1
1	1	0	0	1	0	1	0
1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	0	1

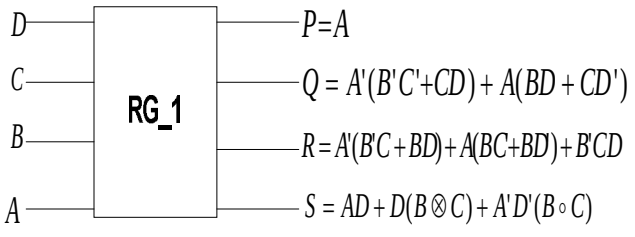


Fig 6. RG_1 Gate

4.1 RELIZATION OF CLASSICAL GATE USING RG_1

When A=0 and B=1, Q=(C D) AND Operation performed
- When A=0 and B=1, CARRY Q=(C D) and SUM
S= (C⊗D), hence we get a Half adder.
- When A=1 and B=1, Q=(C+ D) OR Operation
- When C=0 and D=0, S= (A' B') NAND Operation
- When A=0 and B=1, S=(C ⊗ D) XOR Operation
-When C=1 and B=1, S= (A ⊙ D) NOR Operation

4.2 PROPOSED RG_2 GATE

Table 2 Truth table of Propose RG_2 Gate

INPUT				OUTPUT			
A	B	C	C	X	Y	Z	W
0	0	0	0	1	0	0	1
0	0	0	1	1	1	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0
1	0	0	1	1	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	1
1	1	0	1	0	0	0	1
1	1	1	0	1	0	0	0
1	1	1	1	0	1	1	0

The Truth table of RG_2 Gate is given in Table 2 showing that every input vector has unique output vector, and that no input or output combinations are repeated. As Shown in Figure 7
Inputs= (A, B, C, D)
Outputs= (X, Y, Z, W)
The proposed Gate can be used as AND, OR, XOR, XNOR, Full-Adder and Full-Subtractor.

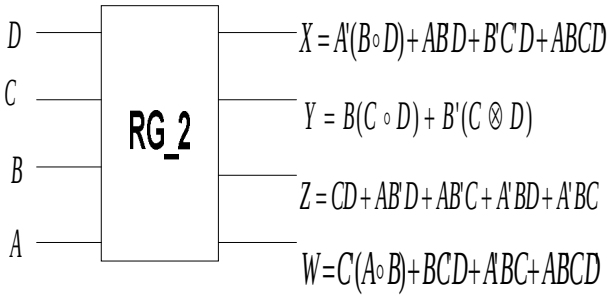


Fig 7. RG_2 Gate

4.3 RELIZATION OF CLASSICAL GATE USING RG_2

-When A=0, B=1, Y= (C⊙D) XNOR Operation.
-When A=1, Y=Difference of B, C, D
Z=Borrow (FULL SUBSTRACTOR)
- When A=0 Sum Y= (B ⊗ C ⊗ D)
Carry Z=B'CD+BC'D+BCD'+BCD for FULL ADDER
-When A=0, B=0, Z=(C D) AND Operation.
-When A=0, B=1, Z= (C+ D) OR Operation.
-When A=0, B=0, X=(C D)'=C'+D' NOR Operation.
-When A=0, B=0, Y=(C ⊗ D) XOR Operation.

5. CONCEPTION OF REVERSIBLE DECODER USING FREDKIN GATE EXPLOITATION

In the Designing of reversible 2 to 4 using Fredkin gate (3*3 Gate). In 2to 4 Reversible decoder total 3 fredkin gate is used market FG1, FG2 and FG3 three input are select 0 and four output marked as OUT0, OUT1, OUT2 and OUT3 and two are garbage output (undesirable output) Garbage output are minimum for good reversible circuit design [5]. One fredkin gate has quantum cost is 5 so in 2to 4 decoder has 3 fredkin gate so total quantum cost is 3*5. As shown in Fig 8.

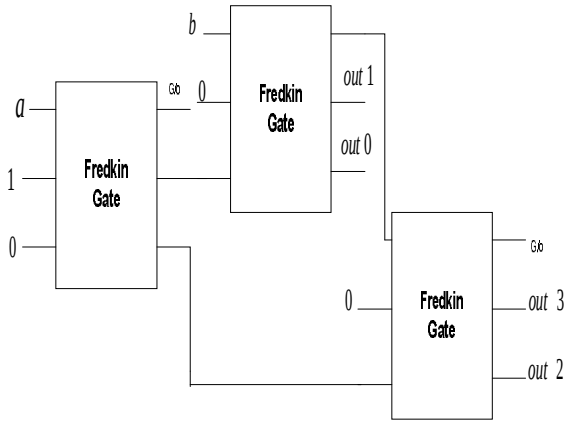


Fig. 8. Schematic of Reversible 2 to 4decoder

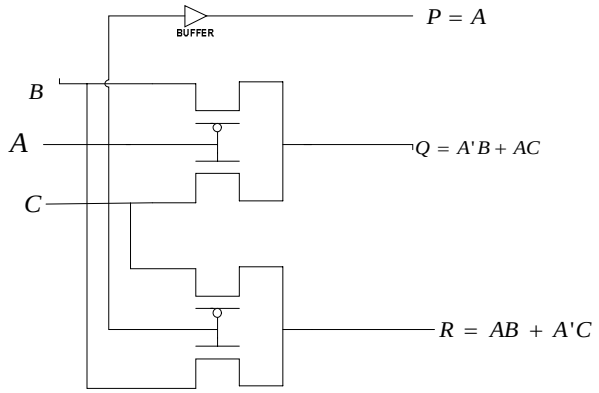


Fig. 9. MOS Implementation of Fredkin Gate.

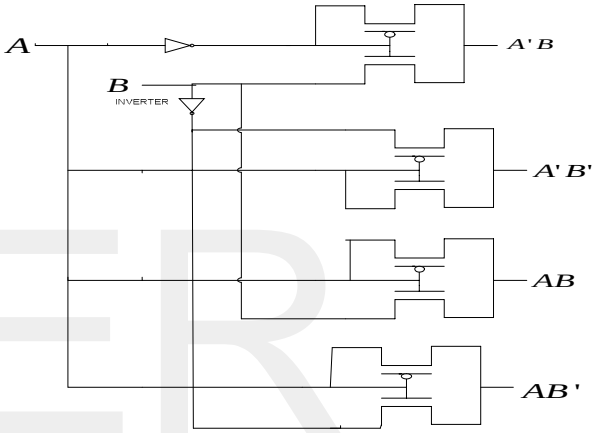


Fig. 10 MOS Implementation of Reversible 2 to 4 decoder using Fredkin Gate.

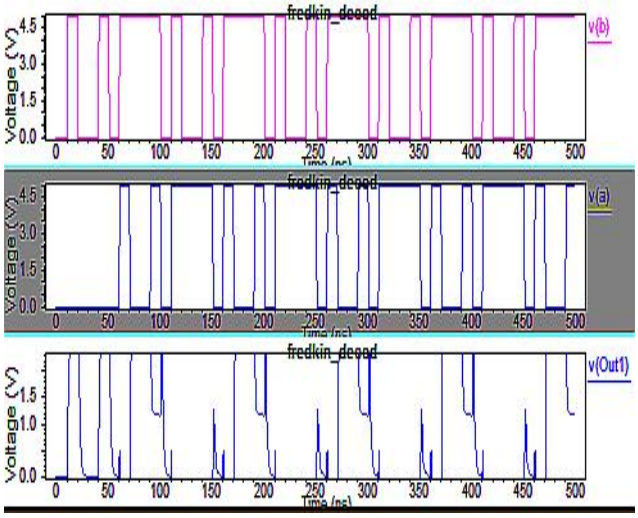


Fig. 11 Simulation Out 1 of Reversible 2to 4 decoder using Fredkin Gate.

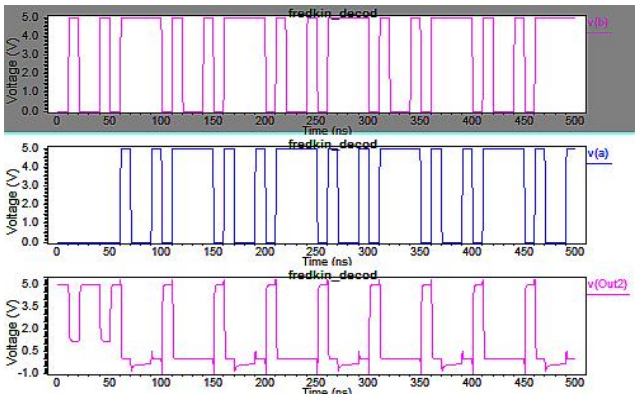


Fig 12. Simulation Out 2 of Reversible 2to 4 decoder using Fredkin Gate.

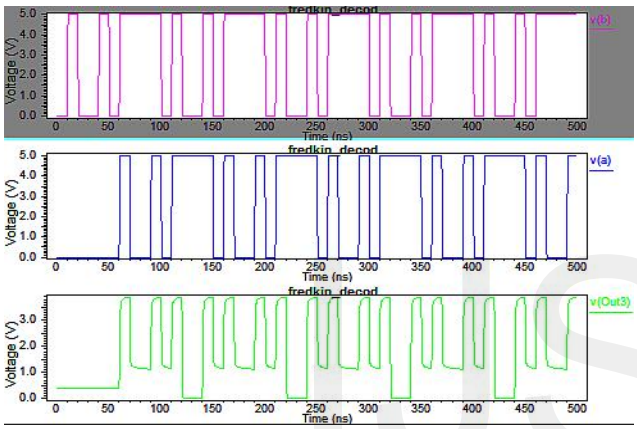


Fig 13. Simulation Out 3 of Reversible 2to 4 decoder using Fredkin Gate.

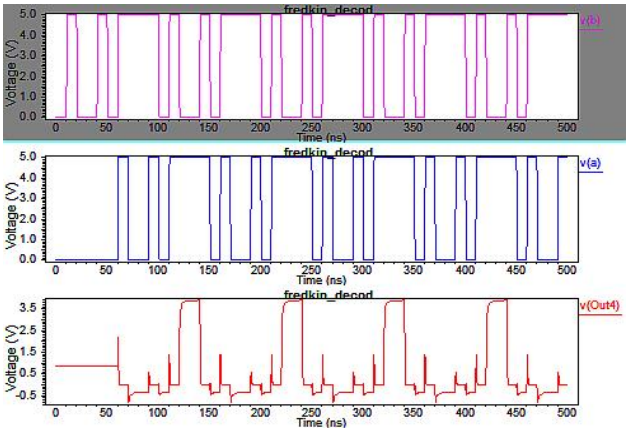


Fig 14. Simulation Out 4 of Reversible 2to 4 decoder using Fredkin Gate.

At temp=0 ^{0}C Power consumption is 1.194519e-003 watts & delay is 5.0211e-008 sec. We are more interest on temperature effect on power and delay we analyze from simulation result as Table 3 shows that at increase temp around 70 ^{0}C power consumption is 1.111972e-003 watts & delay is 5.0273e-008 sec. Means power consumption is decrease by increasing temperature, which is satisfactory factor since Power Consumption is inversely proportional to temperature & delay is increase by increasing temperature, which is also satisfactory factor since delay is directly proportional to temperature. Temperature is important phenomenon for changing parameter like delay, Average Power Consumption etc.

Table 3 Delay and Power at different temperature for 2to4 decoder using Fredkin Gate at 90nm technology node.

V_{DD}=5V	Average Power Consumption (w)	Delay Time (s)	Power-Delay Product (ws)
temp=0 ^{0}C	1.194519e-003	5.0211e-008	5.997754e-11
temp=10 ^{0}C	1.180441e-003	5.0224e-008	5.928646e-11
temp=25^{0}C	1.167736e-003	5.0246e-008	5.867406e-11
temp=40 ^{0}C	1.143824e-003	5.0270e-008	5.750003e-11
temp=55 ^{0}C	1.127373e-003	5.0272e-008	5.667529e-11
temp=70 ^{0}C	1.111972e-003	5.0273e-008	5.590216e-11

Table 4. Simulation results for Reversible 2to4 decoder using Fredkin Gate

Input Voltage (volts)	Average Power Consumption (w)	Delay Time (s)	Power-Delay Product (ws)
0.6	3.0215e-006	2.8433e-010	8.5910e-16
0.8	7.6698e-006	2.7888e-010	21.3895e-16
1	1.3447e-005	2.7374e-010	3.6809e-15
1.2	2.3060e-005	2.6907e-010	6.2047e-15
1.4	3.3724e-005	2.6507e-010	8.8459e-15

We investigate the 2to4 decoder using fredkin Gate from ambient temperature point of view. The rise time, fall time and frequency reported only at the 8.4103e-010, 7.2104e-010and 3.3483e+007at temp 0 ^{0}C for 90nm technology node. However table 4 shows the simulated output can work at other temperature and completely robust to temperature variation. And see the effect of temperature on rise time, fall time and frequency. We analyze from simulated result parameter Rise time increase with increase ambient temperature, fall time decrease with increase ambient temperature and frequency of output signal increase with temperature. It ideas that Reversible 2to4 decoder has a strongly accepted in a vast ambient temperature range. As Table 5

Table 5 Value of Rise time, fall time and frequency at different temperature for 2to4 decoder using Fredkin Gate at 90nm technology node.

V_{DD}=5V	Rise Time	Fall Time	Frequency (Hz)
temp=0	8.4103e-010	7.2104e-010	3.3483e+007
temp=10	8.3376e-010	7.1836e-010	3.3523e+007
temp=25	7.5784e-010	7.1448e-010	3.3660e+007
temp=40	7.0831e-010	7.1063e-010	3.3720e+007
temp=55	7.0963e-010	7.0685e-010	3.3721e+007
temp=70	7.1723e-010	7.0311e-010	3.3721e+007

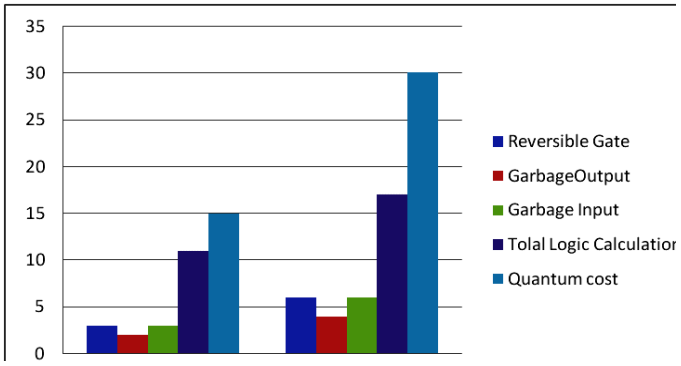
5.1 Calculation of Quantum Cost and Total Logical Calculation for Reversible Decoder

Quantum cost is enumeration the number of primitive gates Thus, the quantum cost of the reversible decoder is more rapidly by varying n where n is number of input and as shown in Table 6

Table 6 Comparison Result of different Reversible decoder using Freddin Gate

Reversible Decoder	2to4 Decoder	3to 8 decoder
Number of RGate	03	06
Garbage Output	02	04
Constant Input	03	06
Total logical Calculation	1*XOR+3NOT+7*AND	12*AND+05*NOT
Quantum Cost	3*Fredkin Gate=3*5=15	6*Fredkin Gate=6*5=30

Chart 1 Shows the Graphical Representation of Table 3



5.2 Simulation Sequel of Reversible 2 to 4 decoder and 3 to8 Decoder using Xilinx Platform

Reversible Decoder is compelled using VHDL (Very High Speed Integrated Circuited Hardware Description Language) code The individual gate operable is flail using Behavioural style of Modelling, the overall logic is follow out Structural style of Modelling[9] more over the FPGA synthesis is done using Xilinx ISE Design Suite 14.5.The Xilinx Vertex 7 XC6vlx75TL package FF484 Speed grade -1L device is found to be the most streamlined in footing of both speed and area and Simulated using Isim. The device contains 46560 slices and 240 bounded input/output pads. The delay for the this finical device is shown in Fig 15 and simulation results are shown in shown in Figure 19 and 20.

```
Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 14 / 6
-------------------------------------------------------------------------
Delay:               1.038ns (Levels of Logic = 3)
  Source:            c (PAD)
  Destination:       out1 (PAD)

  Data Path: c to out1
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5   0.003   0.580  c_IBUF (ga2_OBUF)
     LUT3:I0->O            1   0.053   0.399  out11 (out1_OBUF)
     OBUF:I->O                 0.003          out1_OBUF (out1)
    ----------------------------------------
    Total                      1.038ns (0.059ns logic, 0.979ns route)
                               (5.7% logic, 94.3% route)
=========================================================================
```

Fig 15. Delay for the Reversible 2to4 decoder

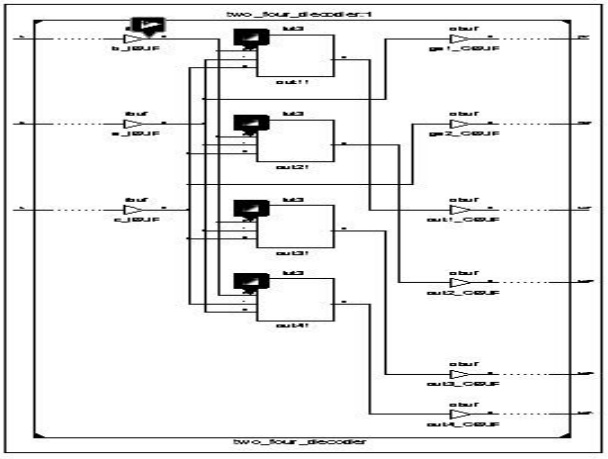


Fig16. Technology Scene of the Reversible 2 to 4 decoder

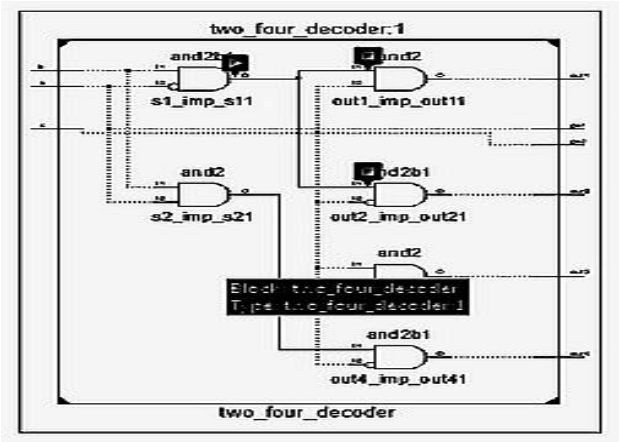


Fig 17. RTL Scene of Reversible Gate Level Realization of 2 to 4

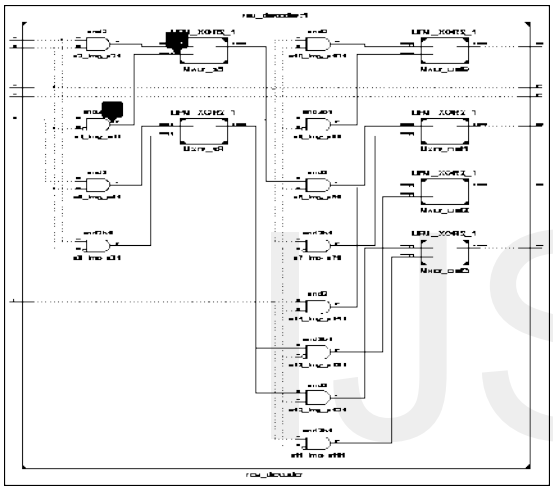


Fig 18. RTL Scene of Reversible 3 to 8 decoder

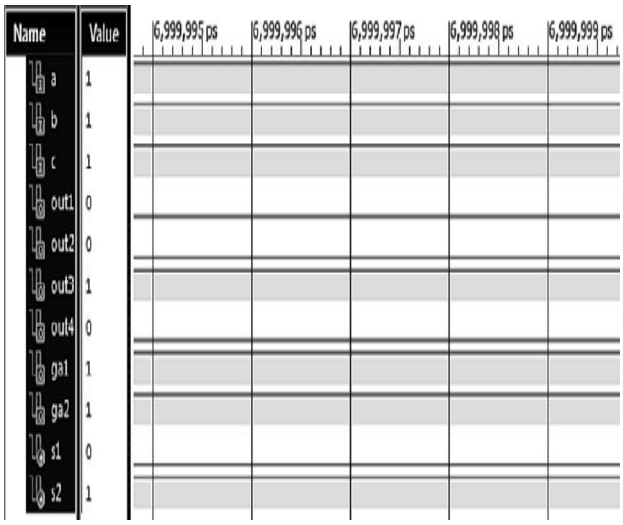


Fig 19. Simulation of Reversible 2to 4 decoder

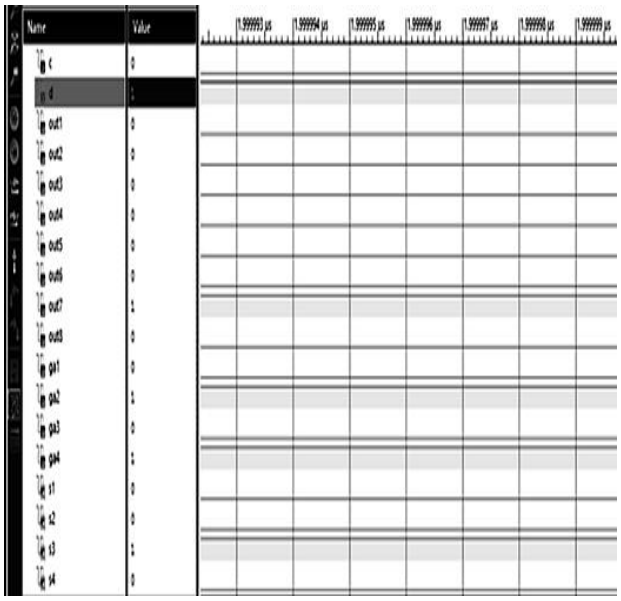


Fig 20. Simulation of Reversible 3to 8 decoder

From the Figure19 and 20 it is prime facie that only one output is high for various input so reversible 2to4 and 3to8 decoder is verified and gives precise output for Digital input
.From the truth table of Reversible 2 to 4 decoder four outputs marked as out1, out2, out3 and out4 for selecting the input D and C and give output as appropriate.

6. SIMULATION DISSECTION BASED ON VLSI TOOL TANNER EDA

Further work can be finished by Tanner tools. Simulation is settled on "TANNER EDA V14" tools technology file used is 90nm.Tanner tools are fully- integrated solution consisting of tools for schematic entry, circuit simulation and waveform probing. The schematic capture of 2to 4 decoder is shown in Figure 21 and the output waveform for 2to 4 decoder is shown in Figure 30. Tanner EDA tools get a more accurate result. Reversible SC Gate marked input in order Iv= (D, C, B, A) where A=1 and B=0 and corresponding output of SC Gate is R and S. These outputs are applied to another SC Gate and selecting first and fourth input is Zero. Out 1 gives output for 2to4 decoder. Output of 2 to 4 decoder is R+S= (D⊙C) + (D⊗C)

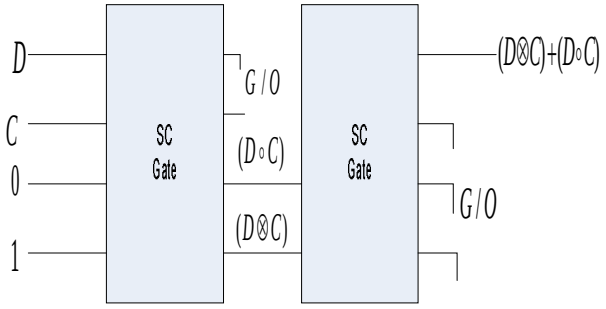


Fig.21 Proposed Reversible SC Gate work as 2to 4 decoder

In Reversible 2to4 decoder gate is realized in transistor implementation [10] as described in Figure 23. To construct reversible decoder MOS transistors are required as on Boolean expression. For Transistor level of these output are implement using Gate diffusion interface (GDI) technique.

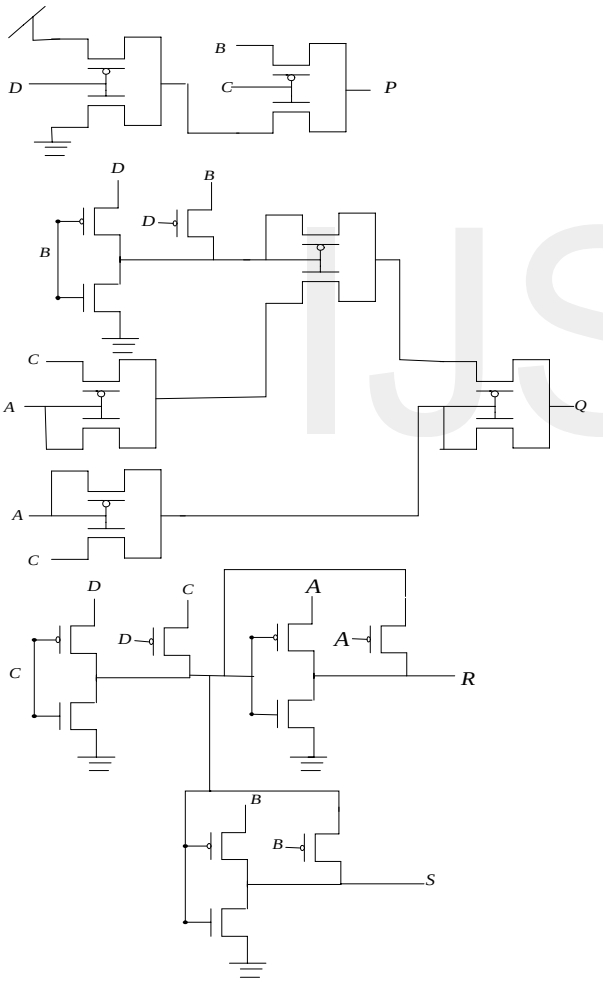


Fig.22 MOS Implementation of SC Gate

In this Gate setting input of SC Gate as A (Value ON=5V, OFF=5V), B (Value ON=0V, OFF=0V) C (Value ON=5V, OFF=0V) and D (Value ON=5V, OFF=0V) and give output R and S these output feed to second SC Gate in this Gate first and fourth input set to Value (ON=0V, OFF=0V) and gives first output for reversible 2to4 decoder. Simulation is done on S-Edit the simulator of S-Edit is T-Spice and waveform is visualized on W-Edit viewer. Simulation output shown in Figure 24.

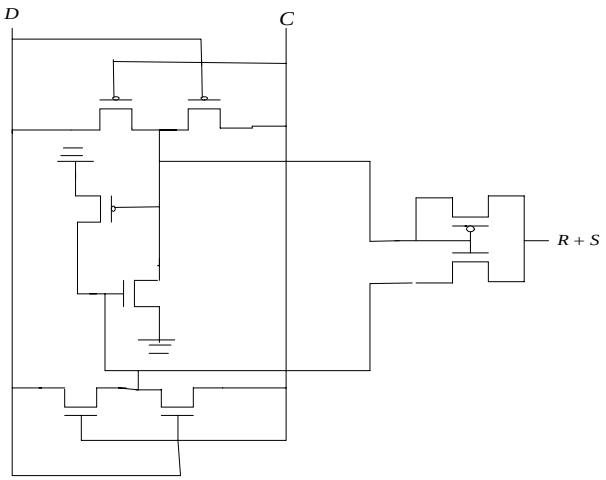


Figure.23 MOS implementation of Reversible 2to4 decoder using SC Gate

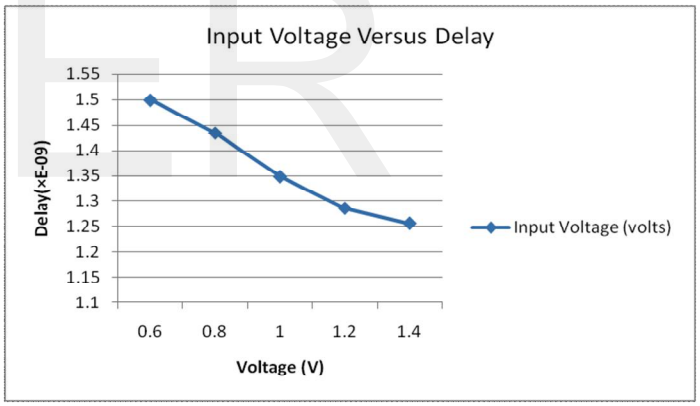


Figure 24 Delay versus Input voltage of SC Gate as 2to 4 decoder

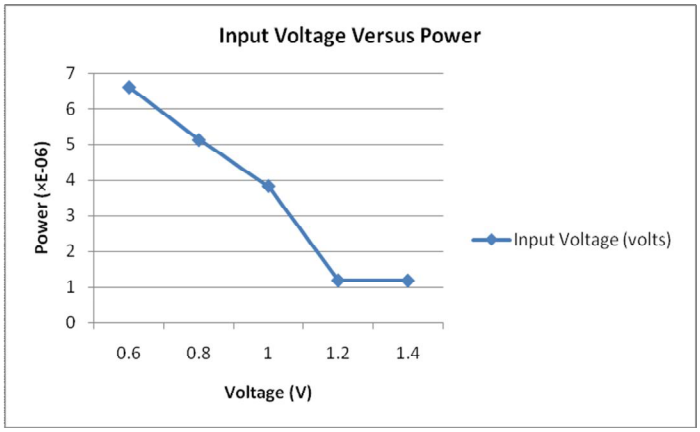


Figure 25 Power versus Input voltage of SC Gate as 2to 4 decoder

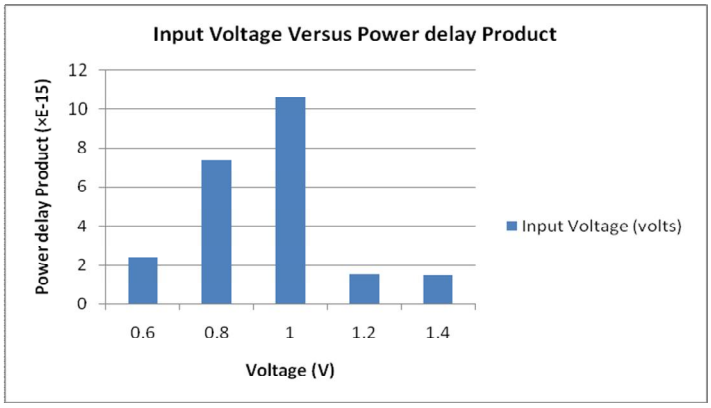


Figure 26 Input voltage versus Power delay Product of SC Gate as 2to 4 decoder

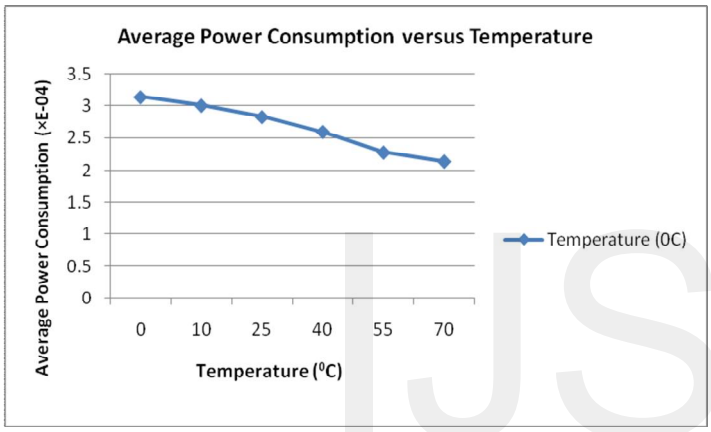


Figure 27 Average Power Consumption versus Temperature of SC Gate as 2to4 decoder

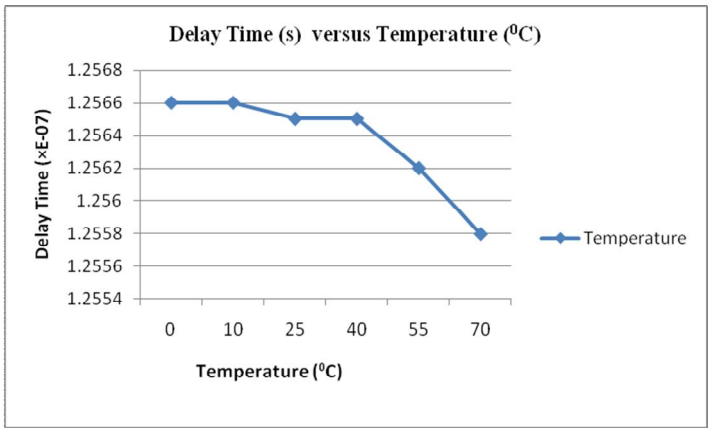


Figure 28 Delay versus Temperature of SC Gate as 2to4 decoder

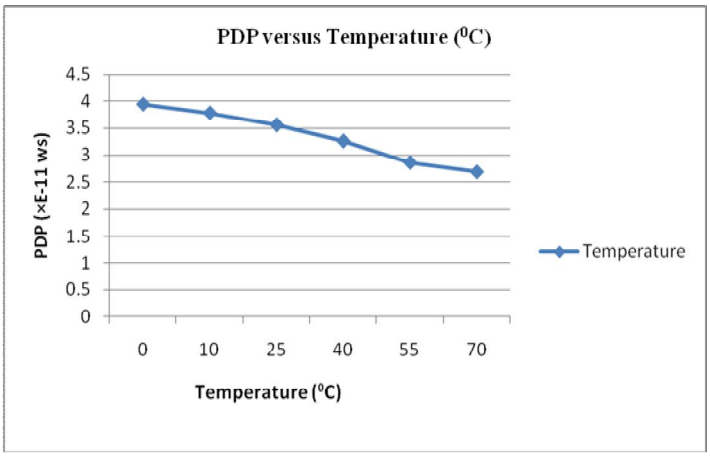


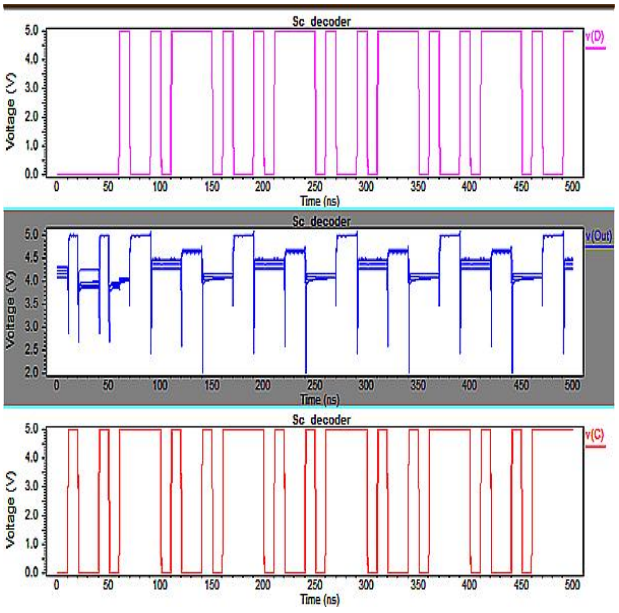
Figure 29 PDP versus temperature of SC Gate as 2to 4 decoder

Table 7 Value of Rise time, fall time and frequency at different temperature for 2to4 decoder using SC Gate at 90nm technology node.

V_{DD}=5V	Rise Time	Fall Time	Frequency (Hz)
temp=0	1.0918e-010	1.5421e-010	1.0000e+007
temp=10	1.0818e-010	1.4526e-010	1.0000e+007
temp=25	1.0702e-010	1.2991e-010	1.0000e+007
temp=40	9.7322e-009	9.8844e-009	1.9983e+007
temp=55	9.8103e-009	9.8450e-009	1.9996e+007
temp=70	9.4996e-011	8.2735e-011	1.0000e+007

Table 8 Power Comparision Analysis of Reversible 2 to 4 decoder using SC and fredkin Gate at V_{DD}=5v

VDD=2V	Reversible 2to4 decoder using SC Gate	Reversible 2to4 decoder using Frekin Gate
AVERAGE POWER (watt)	2.140350e-004	1.161654e-003
MAXIMUM POWER (watt)	1.267326e-002 at time 9.11641e-008	3.468143e-002 at time 2.00565e-007
MINIMUM POWER (watt)	2.774658e-009 at time 1e-008	1.305187e-009 at time 1e-008



Average power consumed=4.449798e-004 watts at V_{DD}=5V

Fig 30. Simulation output of Reversible 2to 4 decoder Using SC Gate

From the Figure 30 of Reversible 2to 4 decoder it is Prime cause that only one Output is high for various input means that Reversible 2to4 decoder is verified and give precise output on Tanner 14 EDA platform.

Table 9 Comparision Result of Reversible decoder 2to4 decoder

Reversible decoder	Transistor Count	Garbage Output	Power dissipaton at V_{DD}=1.8V
Fredkin Gate 2to 4 decoder	14	4	7.561475e-005 watt
SC Gate 2 to4 decoder	8	5	2.105985e-007 watts

7 CONCLUSION

In this Paper we have show an epitome design for reversible decoder. Decoder are more often used for Digital display, digital to analog converter and for memory addressing etc, In Reversible decoder comprise of that in schematization of Quantum cost as canvas to fredkin gate. In 2 to 4 decoder has Quantum cost 15 and single fredkin gate has 5. Future works is promoting improvement in Decoration of Reversible decoder to minimize the Garbage output and total logic calculation.

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